FIG. 1
(PRIOR ART)

FIG. 2A
(PRIOR ART)

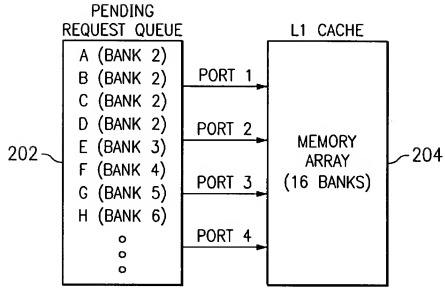
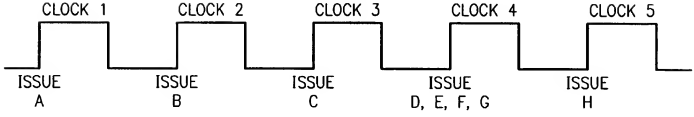
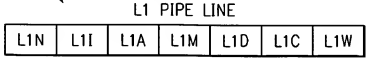


FIG. 2B
(PRIOR ART)



300

FIG. 3



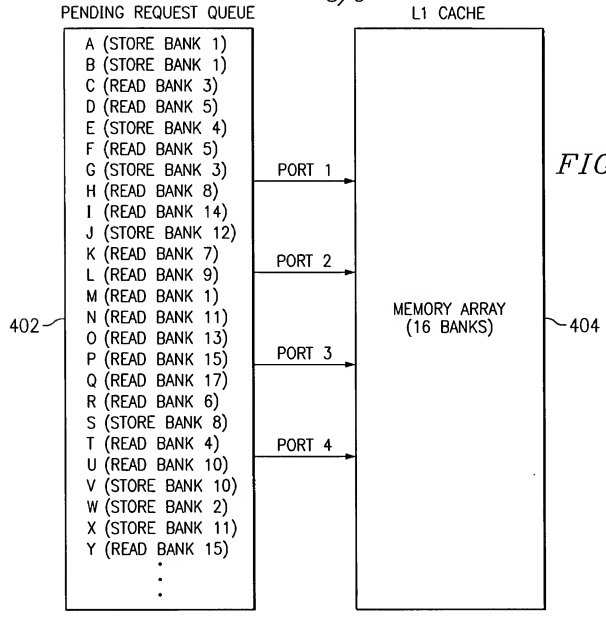

PENDING REQUEST QUEUE
L1 CACHE
A (STORE BANK 1)
B (STORE BANK 1)
C (READ BANK 3)
D (READ BANK 5)
E (STORE BANK 4)
F (READ BANK 5)
G (STORE BANK 3)
H (READ BANK 8)
I (READ BANK 14)
J (STORE BANK 12)
K (READ BANK 7)
L (READ BANK 9)
M (READ BANK 1)
N (READ BANK 11)
O (READ BANK 13)
P (READ BANK 15)
Q (READ BANK 17)
R (READ BANK 6)
S (STORE BANK 8)
T (READ BANK 4)
U (READ BANK 10)
V (STORE BANK 10)
W (STORE BANK 2)
X (STORE BANK 11)
Y (READ BANK 15)
PORT 1
PORT 2
PORT 3
PORT 4
MEMORY ARRAY
(16 BANKS)
402
404

FIG. 4A

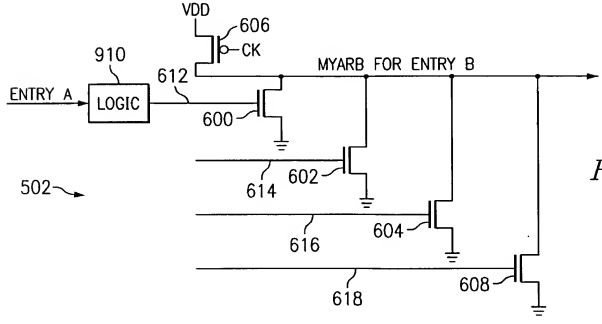

VDD
606
CK
910
612
MYARB FOR ENTRY B
ENTRY A
LOGIC
600
614
602
502
616
604
618
608

FIG. 6

CLOCK 1
CLOCK 2
CLOCK 3
CLOCK 4
CLOCK 5
CLOCK 6
CLOCK 7
L1N=A,C,D,E
L1N=B,F,G,H
L1I =A,C,D,E
L1N=I,J,K,L
L1I =B,F,G,H
L1A =A,C,D,E
L1N=N,O,P,Q
L1I =I,J,K,L
L1A =B,F,G,H
L1M=A,C,D,E
L1N=R,S,T,U
L1I =N,O,P,Q
L1A =I,J,K,L
L1M=B,F,G,H
L1D=A,C,D,E
L1N=M,V,W,X
L1I =R,S,T,U
L1A =N,O,P,Q
L1M=I,J,K,L
L1D=B,F,G,H
L1C=A,C,D,E
L1N=Y,...
L1I =M,V,W,X
L1A =R,S,T,U
L1M=N,O,P,Q
L1D=I,J,K,L
L1C=B,F,G,H
L1W=A,C,D,E
...

FIG. 4B

BANK CONFLICTS RESOURCE OVERSUBSCRIPTIONS ETC
VALID
NEEDL2
504
502
MY ARB GENERATION
506
BYPASSED ISSUED BIT
L1N
508
FIND FOUR IN THIRTY-TWO
ENTRY ISSUED?
ISSUE WORDLINES
510
READ PAYLOAD
ADDRESS AND CONTROL INFORMATION
512
INSERT/X CANCELS
D
Q
S
ISSUED BIT
514
L1I
L1A

FIG. 5

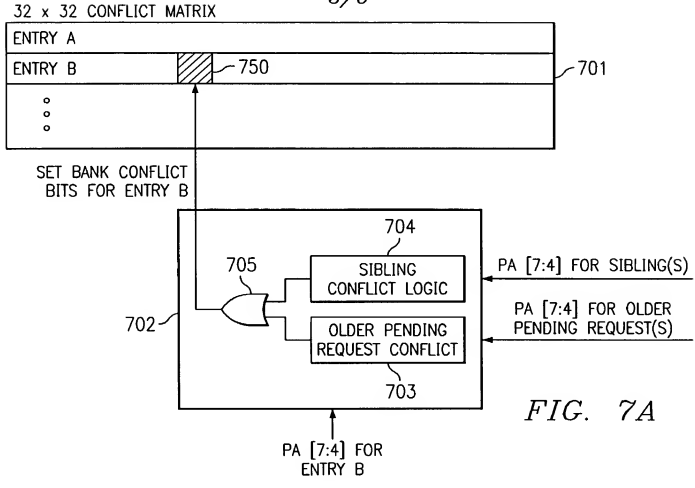

32 x 32 CONFLICT MATRIX
ENTRY A
ENTRY B
750
701
SET BANK CONFLICT BITS FOR ENTRY B
704
705
SIBLING CONFLICT LOGIC
PA [7:4] FOR SIBLING(S)
PA [7:4] FOR OLDER PENDING REQUEST(S)
702
OLDER PENDING REQUEST CONFLICT
703
PA [7:4] FOR ENTRY B

FIG. 7A

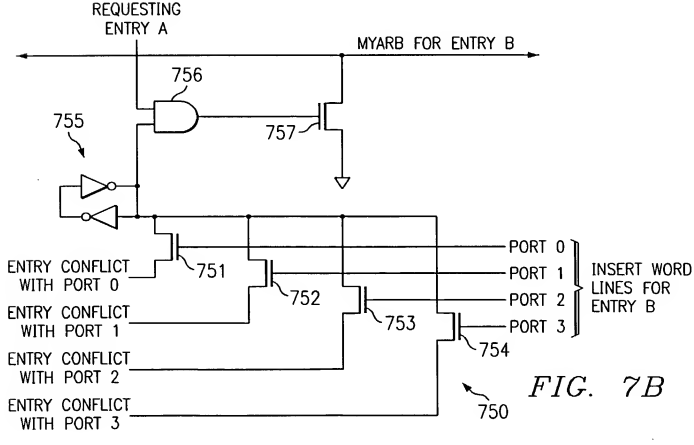

REQUESTING ENTRY A
MYARB FOR ENTRY B
756
755
757
ENTRY CONFLICT WITH PORT 0
751
ENTRY CONFLICT WITH PORT 1
752
ENTRY CONFLICT WITH PORT 2
753
ENTRY CONFLICT WITH PORT 3
754
PORT 0
PORT 1
PORT 2
PORT 3
INSERT WORD LINES FOR ENTRY B
750

FIG. 7B

FIG. 8

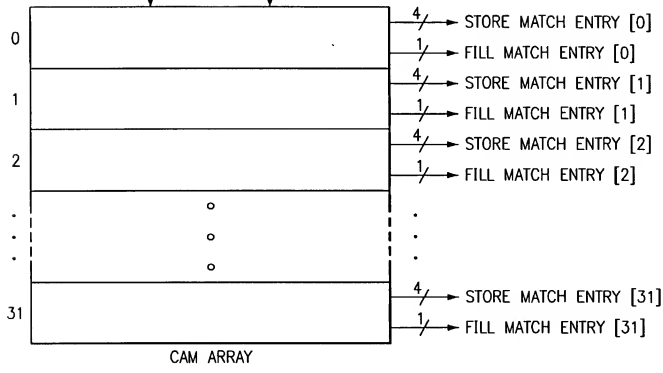
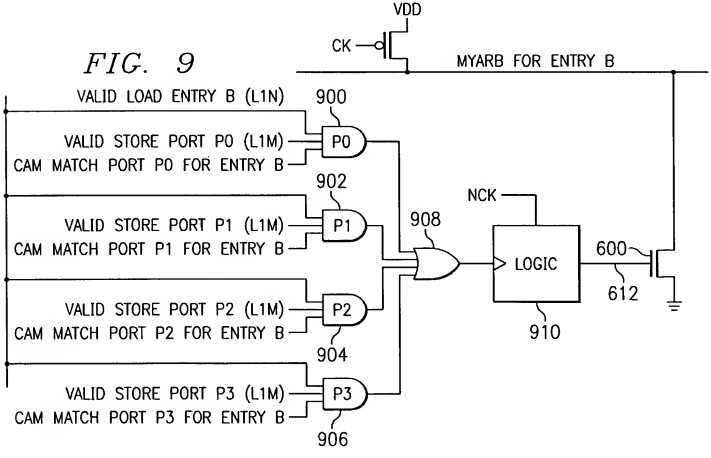

FILL PA[7]
STORE PA[7:4]
1
4
0
1
2
31
STORE MATCH ENTRY [0]
FILL MATCH ENTRY [0]
STORE MATCH ENTRY [1]
FILL MATCH ENTRY [1]
STORE MATCH ENTRY [2]
FILL MATCH ENTRY [2]
STORE MATCH ENTRY [31]
FILL MATCH ENTRY [31]
CAM ARRAY

FIG. 9


VDD
CK
MYARB FOR ENTRY B
VALID LOAD ENTRY B (L1N)
900
VALID STORE PORT P0 (L1M)
CAM MATCH PORT P0 FOR ENTRY B
P0
902
VALID STORE PORT P1 (L1M)
CAM MATCH PORT P1 FOR ENTRY B
P1
NCK
908
LOGIC
600
612
910
VALID STORE PORT P2 (L1M)
CAM MATCH PORT P2 FOR ENTRY B
P2
904
VALID STORE PORT P3 (L1M)
CAM MATCH PORT P3 FOR ENTRY B
P3
906